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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,998	05/12/2001	Tsuruto Matsui	ADV A227.001AUS	6874

7590 03/08/2004

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EXAMINER	
DOOLEY, MATTHEW C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,998	MATSUI, TSURUTO	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2a should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 5 and 6 are objected to because of the following informalities: Following the phrase "defined in Claim 1," the claim is incomplete. A suggested clarification of the claim would read "wherein the semiconductor generates" or "wherein the test system generates" instead of just "generates". Moreover, indentation of the claim would make the claim limitations more identifiable. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 7, and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 discloses a test system for generating test patterns, however nowhere in the limitations of claim 1 is a teaching to a test pattern that is generated, only inversion signal generation. Moreover, there is no teaching as how test patterns will be generated if the memory array does not correspond to the set forth limitations of the row and columns being of different sizes. Claims 7 and 8 also include the aforementioned problems,

specifically no teaching to test pattern generation. Moreover, claims 7 and 8 fail to show how test patterns will be generated if the left and right hand sides of the claimed equation do not equal one another. As such, claims 1, 7, and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura, U.S. 6,523,135.

As per claim 1:

Nakamura teaches to circuitry that includes inversion request signal generation for writing inverted data to specified memory cell locations, wherein the specified memory cell locations are on a diagonal line on an array of memory cells, wherein the number of memory cells in rows and columns are varied (Fig. 1; Col.3: 46 – Col.4: 6; Col.4: 62 - Col.5: 8-14).

As per claim 2:

The internal circuitry of claim 2 functions to bring about the same result as that of Nakamura and as such is not patentably distinct from Nakamura, but is merely an

illustrated design choice for bringing about the identical result. Minor modifications in design between Nakamura and claim 2 do not create patentably distinct inventions, as the circuitry from both systems operates to bring about the same result.

As per claim 3:

Nakamura teaches to pattern generating circuitry that creates includes write data inversion for specified addresses in the memory DUT (Col.3: 46 – Col.4: 6; Col.4: 62 - Col.5: 8-14). The result of the data writing of Nakamura is analogous to that claimed by the claim 3, and as such, claim 3 is not patentably distinct from the system set forth by Nakamura, cited above.

As per claim 4:

Nakamura teaches to pattern generating circuitry that creates includes write data inversion for specified addresses in the memory DUT (Col.3: 46 – Col.4: 6; Col.4: 62 - Col.5: 8-14). The result of the data writing of Nakamura is analogous to that claimed by the claim 4, and as such, claim 4 is not patentably distinct from the system set forth by Nakamura, cited above.

As per claim 7:

Nakamura teaches to a method for generating a test pattern that includes write data inversion for specified addresses in the memory DUT (Col.3: 46 – Col.4: 6; Col.4: 62 - Col.5: 8-14). The result of the data writing method of Nakamura is analogous to that claimed by the method of claim 7, and as such, the method of claim 7 is not patentably distinct from the method set forth by Nakamura, cited above.

As per claim 8:

Nakamura teaches to a method for generating a test pattern that includes write data inversion for specified addresses in the memory DUT (Col.3: 46 – Col.4: 6; Col.4: 62 - Col.5: 8-14). The result of the data writing method of Nakamura is analogous to that claimed by the method of claim 8, and as such, the method of claim 8 is not patentably distinct from the method set forth by Nakamura, cited above.

7. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohsawa, U.S. 6,513,138.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1:

Ohsawa teaches to circuitry that includes inversion request signal generation for writing inverted data to specified memory cell locations, wherein the specified memory cell locations are on a diagonal line on an array of memory cells, wherein the number of memory cells in rows and columns are different from each other (Fig.5, 6; Col. 3: 3-15).

As per claim 2:

The internal circuitry of claim 2 functions to bring about the same result as that of Ohsawa and as such is not patentably distinct from Ohsawa, but is merely an illustrated design choice for bringing about the identical result. Minor modifications in design

between Ohsawa and claim 2 do not create patentably distinct inventions, as the circuitry from both systems operates to bring about the same result.

As per claim 3:

Ohsawa teaches to pattern generating circuitry that creates includes write data inversion for specified addresses in the memory DUT (Fig.5,6; Col.10: 20-34). The result of the data writing of Ohsawa is analogous to that claimed by the claim 3, and as such, claim 3 is not patentably distinct from the system set forth by Ohsawa, cited above.

As per claim 4:

Ohsawa teaches to pattern generating circuitry that creates includes write data inversion for specified addresses in the memory DUT (Fig.5,6; Col.10: 20-34). The result of the data writing of Ohsawa is analogous to that claimed by the claim 4, and as such, claim 4 is not patentably distinct from the system set forth by Ohsawa, cited above.

As per claim 5:

Ohsawa teaches to circuitry that includes address generating circuitry, failure memory, control data, and write data, wherein the write data is sent to a comparator as expected data for comparing with output data from the memory under test (Fig.1, 5, 6).

As per claim 6:

Ohsawa teaches to circuitry that includes address generating circuitry, failure memory, control data, and write data, wherein the write data is sent to a comparator as expected data for comparing with output data from the memory under test, wherein said data contains information on inverted written data (Fig.1, 5, 6; Col.1: 30-35).

As per claim 7:

Ohsawa teaches to a method for generating a test pattern that includes write data inversion for specified addresses in the memory DUT (Fig.5,6; Col.10: 20-34). The result of the data writing method of Ohsawa is analogous to that claimed by the method of claim 7, and as such, the method of claim 7 is not patentably distinct from the method set forth by Ohsawa, cited above.

As per claim 8:

Ohsawa teaches to a method for generating a test pattern that includes write data inversion for specified addresses in the memory DUT (Fig.5,6; Col.10: 20-34). The result of the data writing method of Ohsawa is analogous to that claimed by the method of claim 8, and as such, the method of claim 8 is not patentably distinct from the method set forth by Ohsawa, cited above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.	Osawa et al.	U.S. 5,724,637
b.	Ariki	U.S. 5,925,141

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
03/03/04

Albert DeCady
Primary Examiner